Brief Profile

Name:	Deepak Nagar
Date of Birth:	19-01-88
Educational Qualification:	
Ph. D.	
M. Tech	NITTTR, Chandigarh (Pursuing)
B. Tech	UPTU, Lucknow
Work Experience:	
• *Teaching*	7 Years
• *Research/ Industry/*	-
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Area/Subjects of Interest	Analog Circuits, Digital Electronics
Teaching:	
Subjects Taught at UG level	Electronic Circuits, Digital Electronics
Subjects Taught at PG level	-
Research Guidance	
No. of Ph.D./M.Tech Guided	-
Research Publications	
• Journals	1
• Conferences	-
• Book Chapters	-
Patent/IPR (Books Published etc.)	-
No. of National/International Conferences attended/ Paper Presented	-
STC/FDP/Summer/Winter Schools/Workshops/Seminars attended	-
Memberships of the Professional Societies	-
Awards/Honors	-
Any other relevant Information	Qualified GATE 2011, 2012, 2013.

LIST OF PUBLICATIONS

Journal Papers

1. Rajesh Mehra, Deepak Nagar and Vinayak Yadav, “Effect of Windowing Methods on Performance of FIR filter Design,” in IJSRET Volume 2 Issue 6,pp. 385-388, September 2013.