Brief Profile

Name:	Rohit Lorenzo
Date of Birth:	15-01-1984
Educational Qualification:	
Ph. D. (Full Time)	NIT Silchar (Thesis Submitted)
M. Tech (Full Time)	Karunya University, Coimbatore
B. Tech	UPTU Lucknow
Work Experience:	
• *Teaching -*	8.5 Years
• *Research /Industry*	-
E-mail ID:	rohit.lorenzo@miet.ac.in, rohit.lorenzo@gmail.com
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Area/Subjects of Interest -	Semiconductor devices, VLSI Design , Digital electronics , Analog integrated circuits , Electronic circuits , Low power VLSI Design , VLSI Signal processing , VLSI Technology , ASIC design and VLSI Testing.
Teaching:	
Subjects Taught at UG level	Fundamental of electronic devices, VLSI design , VLSI Technology, Advanced semiconductor devices, Analog Integrated circuits , Electronic Circuits.
Subjects Taught at PG level	VLSI Signal Processing
Research Guidance	
No. of Ph.D./M.Tech Guided	-
Research Publications	
• Journals -	6 (5 SCI + 01 NON SCI)
• Conferences -	15
• Book Chapters –	01
Patent/IPR (Books Published etc.)	-
No. of National/International Conferences attended/Paper Presented	14
STC/FDP/Summer/Winter Schools/Workshops/Seminars attended -	11
Memberships of the Professional Societies	-
Awards/Honors	-
Any other relevant Information	https://scholar.google.com/citations?user=v0IG_e0AAAAJ&hl=nl

LIST OF PUBLICATIONS

Journal Papers

1. Rohit Lorenzo and Saurabh Chaudhury, "LCNT-An Approach to Minimize Leakage Power in CMOS Integrated Circuits," *Microsystems Technologies,* ***springer,*** May 2016. ISSN: 0946-7076 **[SCI].**
   DOI: http://link.springer.com/article/10.1007/s00542-016-2996-y

2. Rohit Lorenzo and Saurabh Chaudhury, "Optimal body bias to control stability, leakage and speed in SRAM cell," *Journal of circuit system and computers*, ***World Scientific,*** Vol. 25, No. 8, pp. 1-15, April 2016. ISSN: 0218-1266**[SCI]**
   DOI: http://www.worldscientific.com/doi/abs/10.1142/S0218126616500961

3. Rohit Lorenzo and Saurabh Chaudhury, "Review of circuit level leakage minimization technique in VLSI circuits," *IETE Technical review*, ***Taylor and Francis,*** April 2016. ISSN: 0256-4602**[SCI]**
   DOI: http://dx.doi.org/10.1080/02564602.2016.1162116

4. Rohit Lorenzo and Saurabh Chaudhury, "Dynamic Threshold Sleep Transistor Technique for High Speed and Low Leakage in CMOS circuits," *Circuit system and signal processing,* ***Springer***. ISSN: 0278-081X **[SCI]**
   DOI: 10.1007/s00034-016-0442-0

5. Rohit Lorenzo and Saurabh Chaudhury, "A Novel SRAM cell Design with a Body-bias Controller Circuit for Low Leakage, High Speed and Improved Stability," *wireless personal communication, Springer*. ISSN:0929-6212 **[SCI]**
   DOI: 10.1007/s11277-016-3788-5

6. Rohit Lorenzo and Saurabh Chaudhury. A Novel Low Leakage body biasing technique for CMOS circuit. *Canadian journal of pure and applied sciences,* vol . 10, issue.1, pp. 3827-3824, Feb 2016.

Book Chapter :

1. Rohit Lorenzo and Saurabh Chaudhury, "Leakage minimization in CMOS VLSI circuits – A brief review" included in book title – Design and modeling of Low power VLSI systems circuit devices and system – IGI global, pp. 71-99, 2016.

Conference Papers:

1. Rohit Lorenzo and Saurabh Chaudhury, "A New body biasing technique for leakage minimization in CMOS VLSI circuits" 4th International conference on computing, communication and sensor network 24-25 Dec 2015.

2. Rohit Lorenzo and Saurabh Chaudhury ,"A New circuit technique to minimize leakage power in CMOS VLSI circuit" 2nd international conference on VLSI Circuit and System , 11-12 July , 2015.

3. Rohit Lorenzo and Saurabh Chaudhury, "Low leakage and minimum energy consumption in CMOS logic circuits" International conference on electronic design computer networks & automated verification 29-30Jan 2015 organized by National Institute of Technology, Meghalaya **.**(IEEE explore)

4. Rohit Lorenzo, Saurabh Chaudhury, Sakshi Devi and Avtar Singh, "Comparative study of Single Gate And Double Gate Fully Depleted Silicon on Insulator MOSFET" Communication, Control and Intelligent Systems , 7-8 Nov 2015. (IEEE Xplore)

5. Rohit Lorenzo and Saurabh Chaudhury, "A Novel body bias controller for low leakage, high speed and improved stability SRAM cell Design" 3rd International conference on computing , communication and sensor network12-14 Dec 2014 organized by Purushottam Institute of engineering and Technology, Rourkela (Odisha).

6. Rohit Lorenzo and Saurabh Chaudhury, "A New Ultra low leakage and high speed technique for CMOS circuits" Students conference on engineering and Systems 28-30 May 2014 organized by Motilal Nehru National Institute of Technology, Allahabad (UP**).** (IEEE explore)

7. Rohit Lorenzo and Saurabh Chaudhury, "A Novel PMOS Data Retention Leakage Power Reduction Design" Proceedings of International conference on communications systems and Network Technologies 7-9April 2014 organized by National Institute of Technical Teachers Training & Research ,Bhopal (MP).(IEEE explore)

8. Rohit Lorenzo and Saurabh Chaudhury, "Analysis of leakage feedback techniques" Proceedings of International conference on Electronics communication and Instrumentation 201416-17 January 2014 organized by Heritage Institute of Technology, Kolkata (WB**).** (IEEE explore)

9. Rohit Lorenzo and Saurabh Chaudhury, "A Novel all NMOS leakage feedback with data retention technique" Proceedings of IEEE sponsored International conference on Control, Automation, Robotics and Embedded system 16-18December 2013 organized by PDPM IIITDM Jabalpur (MP**).** (IEEE Explore)

10. Rohit Lorenzo and Nikhil Raj, Page no. 453-457"An Effective Design Technique to Reduce Leakage Power" Proceedings of IEEE conference on Electrical , Electronics and Computer Science,1-2 march 2012 organized by Maulana Azad National Institute of Technology ,Bhopal (MP). (IEEE Explore)

11. Rohit Lorenzo and O.P.Sahu "A New Approach to reduce Power Dissipation in BIST" in International conference on Communication , Computers and Devices, ICCCD , 10-12 December 2010 Organized by department of Electronics And Electrical Communication **,** IIT Karaghpur (West Bengal)

12. Rohit Lorenzo "Design of a low static power CMOS circuit" Proceedings of National Symposium on Instrumentation -36, 20-23 Oct 2011 jointly organized by INSTRUMENT SOCIETY OF INDIA, Department of Instrumentation, IISc Bangalore and Invertis University, Bareilly.

13. Rohit Lorenzo and O.P Sahu page no. 161-164, Minimum Switching Activity in BIST, Proceedings of National Conference on VLSI , MEMS & NEMS ,VMN'10 ,23-24 September 2010 , Amity University, Noida (UP) India.

14. Rohit Lorenzo ,Tarun Dubey and O.P Sahu , Self Localization Method of Wireless Sensor Network , 5 April 2009 , National Seminar on Wireless Sensor Network ,SRMSCET ,Bareilly (UP),India.

15. Rohit Lorenzo and Amir Anton Jone, VL. 19 , page no.95-98 ,A BIST for Low power dissipation, Proceedings of National Conference on VLSI for Communication ,Computation and Control VCCC'08 , 15 March 2008 , Karunya University ,Coimbatore (TN),India.